Dec 21

Synthesizer Driver

Including Basic AO Modulator Alignment

Instruction Manual

iSK3L (iSA) series RF Synthesizer

iSK3 (iSPA) series RF Synthesizer and Amplifier

iSL3 (iSPH) low cost RF Synthesizer and Amplifier

Applies to Isomet Synthesizer Tool version 2.47 on

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Revision History

22-11-13:	Non-zero RSRR / FSRR Delta-T values	Page 12
07-11-14:	Map settling time	Page 16
15-09-16:	G-Bias control	Page 10
15-09-16:	ADC tab	Page 9
31-07-20:	Add iSH case style	Page 25
31-07-20:	Add basic AOTF set-up	Page 29
10-12-21:	Change of Model Numbers	

GENERAL

The iSK3 (iSA) range of configurable RF drivers is based on a multichannel DDS (synthesizer) and 32-bit ARM microcontroller (uC). The uC contains non-volatile FLASH memory for program storage. This enables the desired operating characteristics to be loaded at power-on without user intervention. The uC also provides diagnostic and house keeping capabilities.

The Isomet Synthesizer Driver Tool v2.47 (or later) software allows PC control of the driver functions using slider and/or key stroke input. The default resolutions are; frequency 0.001MHz, amplitude 0.01%, and phase 0.01°. (Phase control applies to the multi-outputs models).

Former Model No.s

Model	Outputs	Reference Output ⅄	Freq' Doubled	Freq Range (MHz)	RF Output Power
iSA-SF1	1	✓	×	20-200	1mW
iSA-SF1-e	1	✓	✓	40-400	1mW
iSA-SF2	2	×	×	20-200	1mW
iSA-SF2-e	2	×	✓	40-400	1mW
iSPA-SF1 (- w)	1	✓	×	20-200	1.2W*
iSPH-1-w	1	✓	×	20-200	1.2W*
iSPA-SF1-a	1	✓	×	30-60	4W
iSPA-SF1-b	1	✓	×	60-100	4W
iSPA-SF1-c	1	✓	×	80-130	4W
iSPA-SF1-d	1	✓	×	125-175	2W
iSPA-SF1-e	1	✓	×	150-300	2W
iSPA-SF2	2	×	×	20-200	1.2W*
iSPA-SF2-e	2	×	✓	40-400	0.5W
iSPA-MF4	1	×	×	60-160	1W
Generic	-	-	×	10-200	-

* Output power >1.2 W from 20-150MHz (>750mW from 150-200MHz)
(iSPA-SF1 set-up also applies to custom single output high power synthesizer-amplifier combinations)

⅄ Low level reference output (< 800mVpp, 50Ω) at the same frequency as the main output.

Other options:

- E : external temperature monitor / interlock input
-W : water cooled heatsink

Revised Model Numbers

Model			Frequency range	RF output power
iSK3 -	100T - 1	- 1	20-200 MHz	1.2 W
	36T - 1	- 4	24-48 MHz	4 W
	45T - 1	- 4	30-60 MHz	4 W
	60T - 1	- 6	45-85 MHz	6 W
	80T - 1	- 4	60-100 MHz	4 W
	105T - 1	- 4	80-130 MHz	4 W
	150T - 1	- 2	125-200 MHz	2 W

These drivers are designed to operate with a wide range of Isomet AO modulators, low resolution deflectors, tuneable filters and frequency shifters. A block diagram is shown in Figure 5.

The driver may be pre-programmed by the user for autonomous operation or directly controlled via USB connection to a host computer. External controls are applied through a 25 way D-type connector. The external inputs are not necessary to operate the driver.

On power-up or after a *RESET*, the uC configures the direct digital synthesizer (DDS) chip and loads a defined frequency / phase / amplitude profile ('MAP') stored in FLASH memory.
This memory may store up to 8 MAP's (MAP0…MAP7). The driver defaults to MAP0 on power up.

On dual channel models, both outputs are derived from a common reference frequency. The differential frequency shift is therefore highly stable making this unit ideally suited to heterodyne applications.

The driver can be easily programmed to output sweeps or step changes in frequency or phase or amplitude

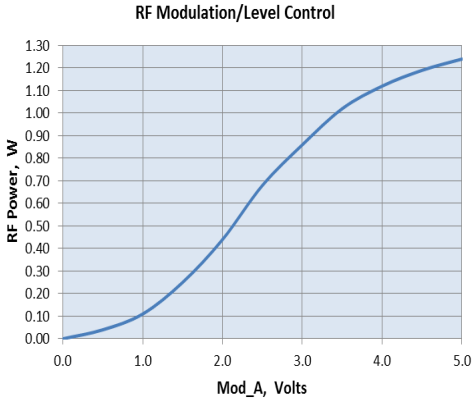
There are four independent methods for output power control.

- ***AMPL*** slider (re: ***Channel*** tab). Provides 10 bit scaling of the DDS output.
  (Note: This slider is inactive during frequency/phase sweep modes.)

- ***Current*** options (re: ***Channel*** tab). Sets the full scale DDS output current.
  Four step increments: Eighth(min), Quarter, Half, *Full*(max).

- Digital pot's (re: ***IO*** tab, ***DAC Wiper Control***).
  Two wipers, ***LVL-D*** and ***LVL-1*** provide preset level control.
  LVL-D sets the DDS output current bounded within the ***Current*** limit.
  LVL-1 sets the power amplifier gain.

- External 0 – 5V input applied to pin 6, 25way D-type connector.
  This can be used for high speed dynamic amplitude control and allows RF modulation to be synchronized with connected equipment.



Typical full power response at 80MHz

RF rise fall/time < 50nsec

DC Power Supply

The operating voltage is +24Vdc at a current drain of approximately < 0.7A. The external power source should be regulated to ± 2% and the power supply ripple voltage should be less than 200mV for best results. Higher RF output power is achieved at 28Vdc.

Air cooling

Free air circulation is required over the driver heatsink.
Fan assist is recommended.
If the internal driver temperature exceeds 50ºC, a warning signal is generated and LED 'F' flashes.

The driver heatsink temperature must not exceed 70°C.

PRECAUTIONS

LVTTL digital input levels must not exceed **3.3 volts**

Analog input levels must not exceed **12 volts**

DAMAGE TO THE AMPLIFIER MAY RESULT IF THE TEMPERATURE EXCEEDS 70°C.

SERIOUS DAMAGE TO THE AMPLIFIER MAY ALSO RESULT IF THE MAIN RF OUTPUT(S) IS OPERATED OPEN-CIRCUITED OR SHORT-CIRCUITED. (Reference outputs may be left un-terminated)

Example uses:

- High stability tuneable differential frequency source for Heterodyne applications using AO frequency shifters.
- High stability tuneable source for Spectroscopy applications using AOTFs
- Bidirectional or unidirectional frequency sweeps for laser scanning applications using AO deflectors

1. OPERATION

The manual will first describe basic single tone operation using no external control inputs.
Subsequent sections will describe sweep modes, profile select, external control and storage features.

Before operating the driver, always terminate the main RF output(s) with an AO device or 50Ω load.
Connect the DC supply (refer section 3).

1.1 Install Software.

Run the ***setup.exe*** from the iHHS Tool directory
Select and run ***Isomet iHHS Tool*** from the Start Menu, All Programs.
Connect the USB and apply DC power (+15V minimum, +28V maximum)

The title bar will show ***Connected*** and the firmware version (e.g. v02.06) once USB communication is established. The Isomet GUI features tooltip hints. Place the cursor near a wiper or check box to display the corresponding Tooltip.

The driver will only respond to data changes after the ***Write*** button at the foot of each page is pressed. Slider controls are one exception. Selected data is auto-written once the respective slider button is released. The ***Write*** button can also be used to confirm new slider values.

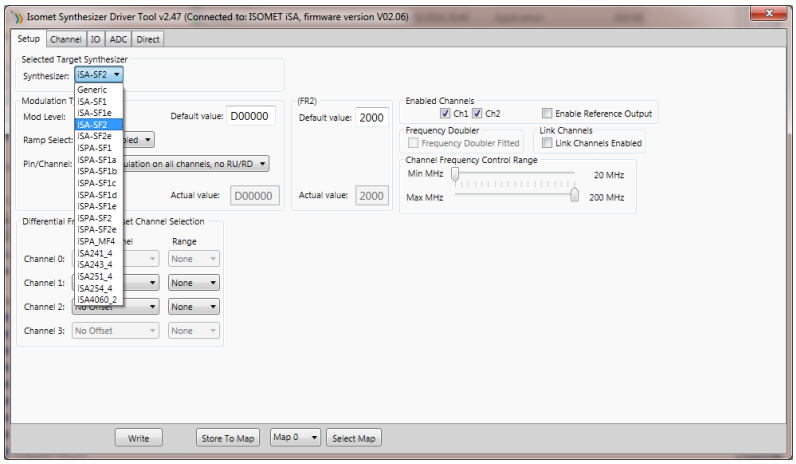
The slider controls snap to the nearest 0.5 unit. Fine control is achieved using the navigation keys.

Keys	FREQ slider	PHASE slider	AMPL slider
+ / -	1 MHz	10 °	10%
PgUp / PgDn	0.1 MHz	1 °	1%
↑ / ↓ arrows	0.01 MHz	0.1°	0.1%
← / → arrows	0.001 MHz	0.01°	0.01%

The opening window will display four menu tabs. ***Setup, Channel, IO*** and ***Direct.***
The ***Direct*** tab displays internal register values and is a low level diagnostic tool.
(Please refer to the Analog Devices AD9959 data sheet for detailed explanation)
Most user controls are found under the ***Channel*** and ***IO*** tabs

1.1.1 Select Model

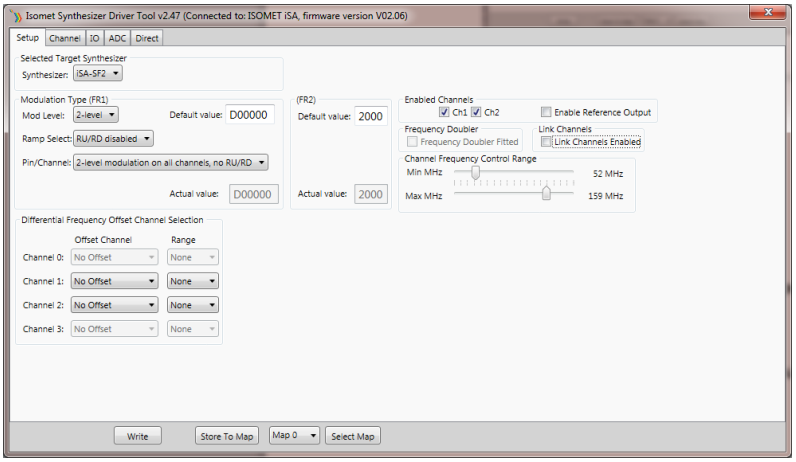
Use the ***Synthesizer*** drop down menu to select the specific iSA or iSPA model.
Use tables page 3 to cross reference for an iSK3 model.
This will configure the GUI to suit the hardware



Certain models contain frequency doublers to extend the frequency range up to 400MHz. This option is factory fitted. The GUI allows for the multiplication provided the correct model is specified.

1.2 Single Tone Mode

a) The ***Setup*** tab allows the user to select the operating mode and set global limits.



For basic single tone (static frequency) operation, use the default values for the ***Modulation Type (FR1)*** and ***(FR2)*** panels as shown above.

Channel Frequency Control Range panel
Set the min-max limits for all frequency input controls.

Enabled Channels panel

In all cases one or more channels MUST be selected, depending on the model

iS(P)A-SF1: Check Ch2 box.
iS(P)A-SF2: Check Ch2 and / or Ch1

Some driver models are fitted with a low level reference output(s). These are enabled by checking the ***Enable Reference Output*** box.

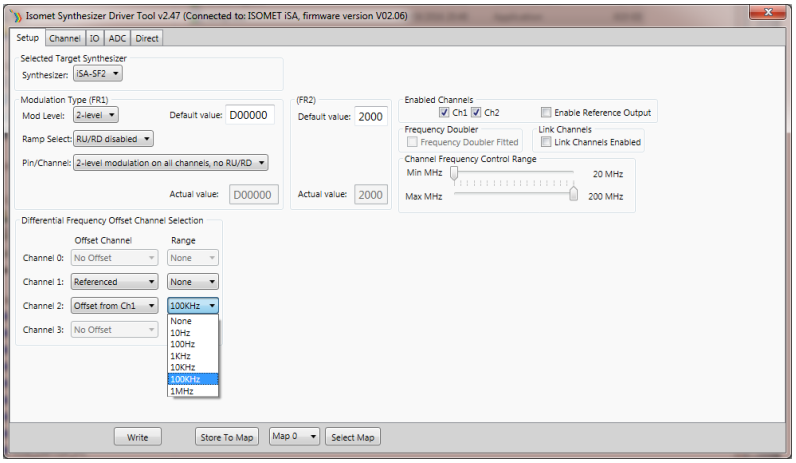
Link Channels ☐ check box
When checked, this links all four channels to together. (The ***Enabled Channels*** check boxes will be greyed out) Channels Ch1 and,2 will output exactly the same Frequency, Amplitude and Phase (F/A/P) values. Ch1 becomes the master. The value(s) set on Ch1 will be applied to the slave channels Ch2. Values on the Slave channels may be subsequently altered.

Link Channels only applies to single tone operation, (see Section 6, Channel Tab).
[Don't forget, press ***Write*** to load new values]

Differential Frequency Offset Channels Selection panel

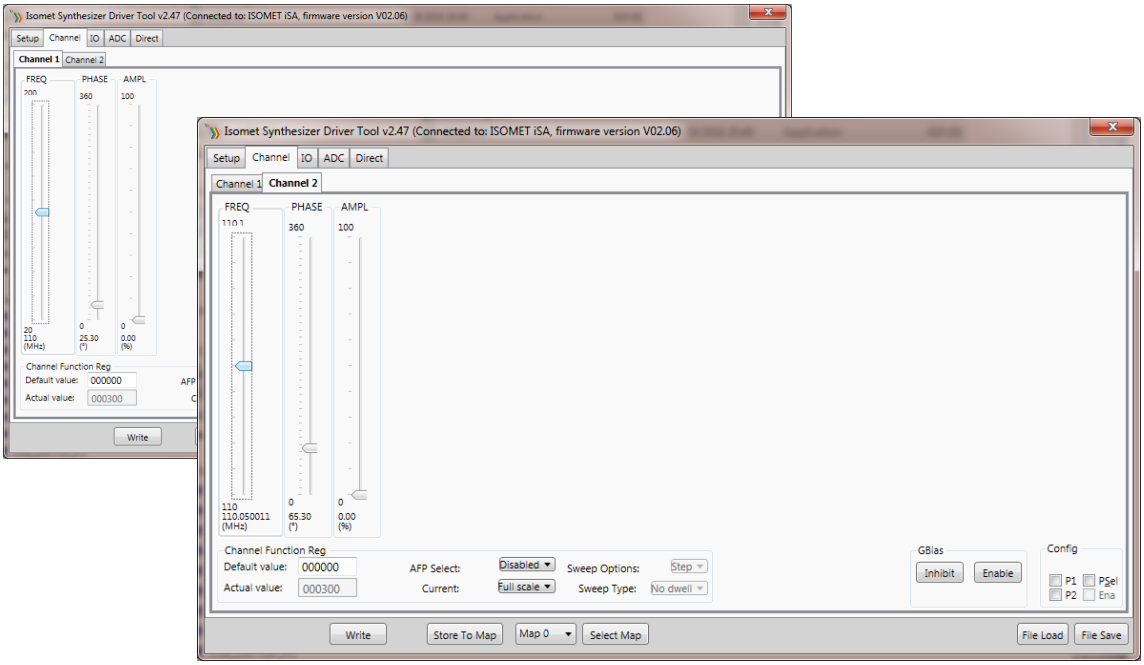
When a small frequency difference between 2 channels is required this panel allows the user to select a reduced adjustment range on one channel with respect to the selected master channel

e.g. 100kHz range on Channel 2 with respect to Channel 1
Select the Offset Channel 2 and full range limit of 100KHz

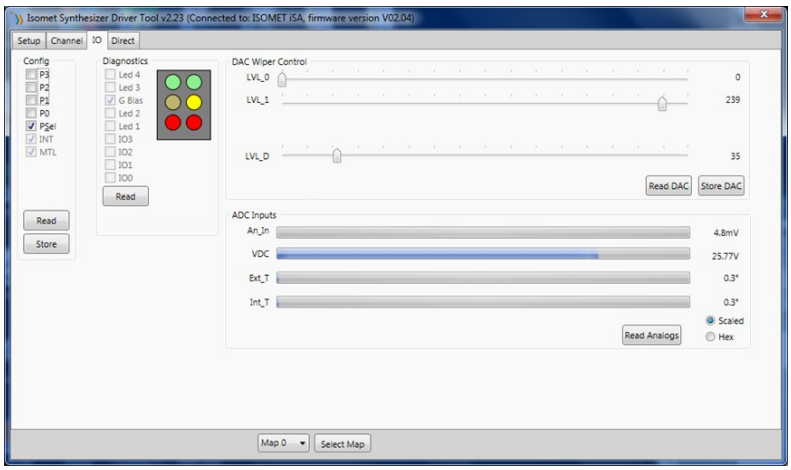


Use Channel slider tabs to set the frequency (also refer to page 11)

- First: Set the master Channel 1 = 110.0000 MHz
- Second: Set the offset frequency on the slave Channel 2 = 110.050011 MHz



Tip: For precise control, set the Channel Frequency sliders to minimum using the mouse and then use the arrow keys to increment (see table page 6)
The ***IO*** tab allows the user to set output amplitude and view sub set of the diagnostics (full diagnostics on ***ADC*** tab).



DAC Wiper Control panel:
The default settings give maximum output.

- ***LVL_D*** sets the DDS chip output current, maximum on LH side (0)
  This wiper controls both the main and reference RF output levels.

- ***LVL_1*** sets the amplifier gain, maximum on RH side (255)
  This wiper controls only the main RF output level.

- ***LVL_0*** reserved for future use.

ADC Inputs panel:

- ***An-In***: Measures the voltage applied to pin 5 on the 25way D-type connector (Max +10V)

- ***VDC***: DC voltage applied to iSA-SF

- ***Ext_T***: (Option). Displays the temperature of external equipment fitted with an AD590 sensor circuit.

- ***Int_T***: Displays the temperature of the iSA-SF heat sink

Config panel: The profile inputs [P0…3] are multi-purpose. Their function depends on the operating mode. Not used for basic single tone operation.

Diagnostic panel: Not required for basic operation. See section 2.7 for LED explanation

[Don't forget, press ***Write*** to load new values]

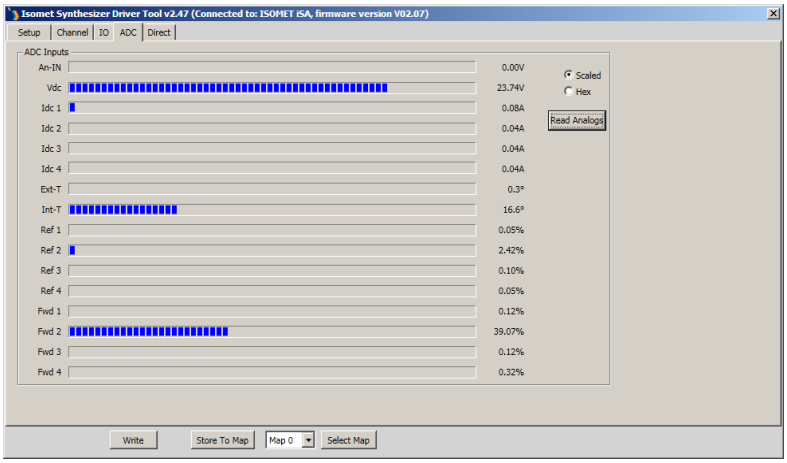
b) The ***ADC*** tab is display diagnostic measures.

An-In: Measures the voltage applied to pin 5 on the 25way D-type connector (Max +10V)
Vdc: Indicates supply voltage at the RF driver (+/- 5%)
Int_T : Indicates temperature of RF driver heatsink

The following only applies if the diagnostic signal are supported by the connected AO device or integrated power amplifier:

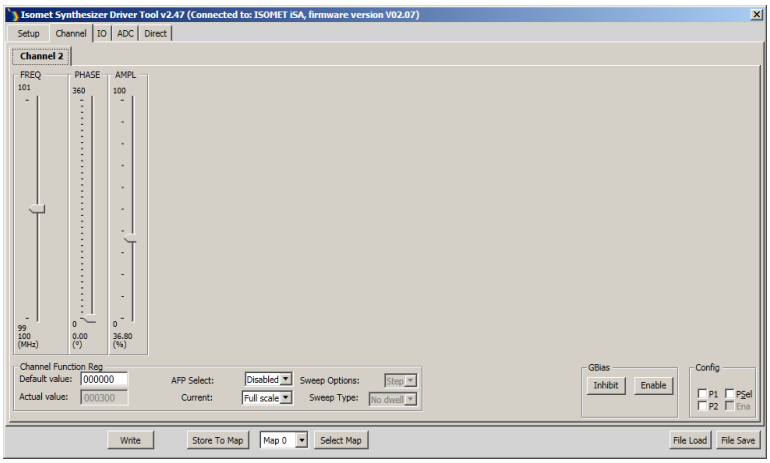
Ext_T: Indicates temperature of the AO device
Ref n: reflected RF power of Channel n
Fwd n: forward RF power of Channel n

These are not a quantitative measure but do provide a indicative level.



[Press ***Read Analogs*** to load and update values]

c) The ***Channel*** tab allows the user to set the RF output characteristics.



Note: Only the channels enabled under the ***Setup*** tab will be displayed

Use the sliders to set the output frequency, phase and amplitude scaling.

Each channel is set independently. Select the appropriate **Channel 1** or **Channel 2** slider group tab.

Once the desired values have been written to the iSA / iSPA, these can be stored into MAP0 and will become the new default values on power-up.

[Don't forget, press ***Write*** to load new values]

Press the ***Store to Map*** with ***MAP0*** showing in the adjacent pull down menu

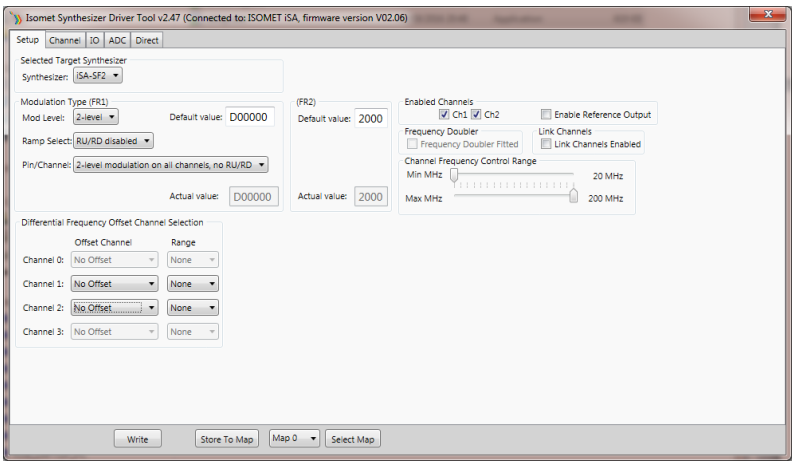
This window also includes the G-BIAS buttons ***Inhibit*** and ***Enable***
These can be used to turn the RF power Off and On for higher RF power models that support this feature.

This completes the basic driver configuration.

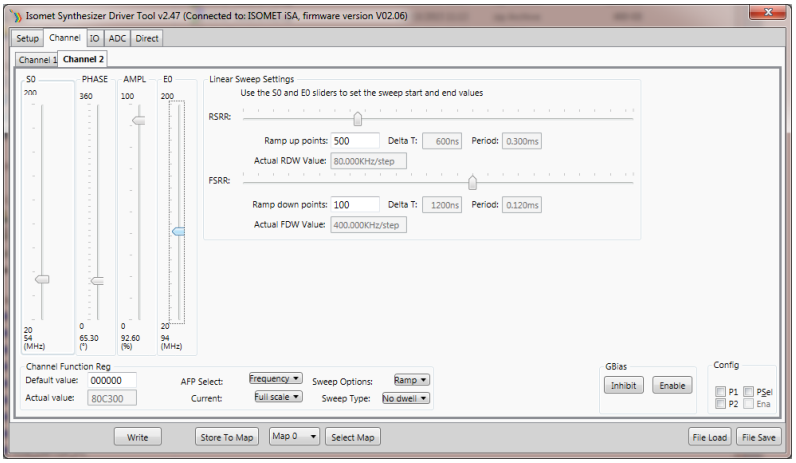
Refer to Section 4 for AO alignment

2.3 **Sweep Mode.** Typical mode for AO Scanning applications

a) To enable frequency, phase or amplitude sweep modes, the ***Mod Level*** under the ***Setup*** tab must be set to ***2-level***



b) The sweep modes are selected under the ***Channel*** tab.



In the screen shot above, a frequency ramp is selected.
Start sweep (S0) 54MHz, End sweep (E0) 94MHz.
Rising slope 300us total duration, 500 points, falling slope 120us and 100 points
Full scale amplitude selected. Ramp mode, No dwell. Explanation below

AFP Select pull down menu selects the parameter to be swept; Amplitude, Frequency or Phase
The fundamental slider is assigned the start value and an additional slider is displayed to set the end value.

Sweep Options pull down menu selects the sweep mode;

- ***Step*** is an instantaneous shift between two selected points.
- ***Ramp*** is a series of incremental steps between the start (S0) and end (E0) values.

Sweep Type pull down menu selects the sweep characteristic for the RAMP mode only ;

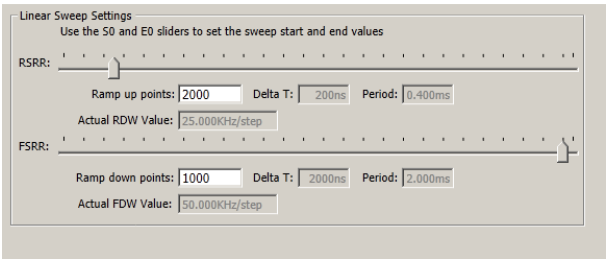
- ***No Dwell***: output returns to the start value immediately the end value is reached.
- ***Dwell***: output ramps up on the +ve edge and down on the –ve edge of the control input P2 (P1)

[Don't forget, to press ***Write*** to load new values]

c) ***RAMP mode.*** Generates a linear uni or bi-directional sweep.

May be applied to either Frequency or Phase.
(A limitation in the DDS chip prevents an amplitude ramp in this mode).

An addition panel is displayed allowing the user to program the rising and falling ramp characteristics.

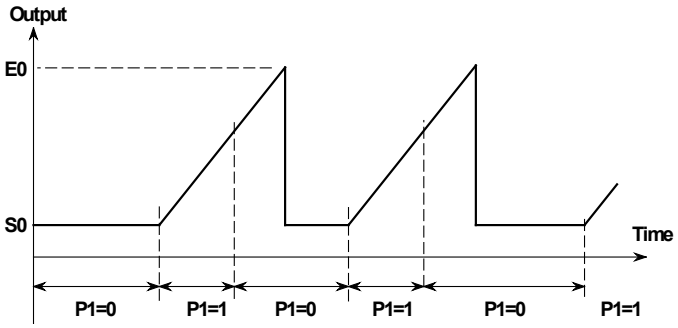


The *RSRR* slider defines the duration of the rising slope increment.
The value is displayed in the *Delta T* window
The number of rising ramp points are entered into the ***Ramp up points*** window.
The total rising ramp time is displayed in the *Period* window.

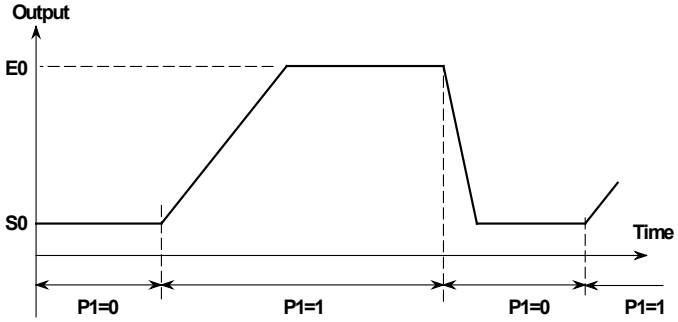
FSRR slider defines the duration of the falling slope increment.
The falling slope only applies if ***Dwell*** is selected in the ***Sweep Type*** pull down menu.

For correct initialization, please ensure non-zero values in BOTH Delta T windows
(e.g. move slider at least 1 tick)

A ***No-Dwell*** sweep immediately returns to the S0 start value after the end value E0 has been reached



A ***Dwell*** sweep only returns to the S0 start value after a falling edge transition on the appropriate profile input



(Both plots show a Ch1 ramp, controlled using input P1)

The sweep is initiated by toggling the profile input (P0..3) associated with the selected channel.
All the Profiles Inputs are displayed in the ***Config*** panel under the ***IO*** tab and a sub-set is repeated under the ***Channel*** tab

P1 = Channel 1 sweep control
P2 = Channel 2 sweep control

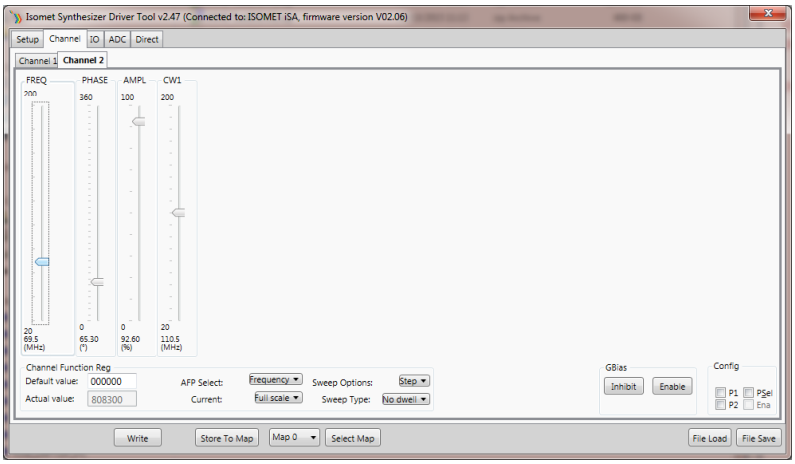
Check box ***Psel*** selects the source of the P1 and P2 sweep control inputs.

Psel checked (high), selects external P1/P2 inputs on the 25way D-type (see page)
Psel unchecked (low), selects USB/PC control of ***P1*** and ***P2*** check boxes, shown in the ***Config*** panels of this GUI.

When using the ***Config panel*** under the ***Channel*** tab, be sure ***Psel*** is unchecked under the ***IO*** tab.
Press ***Read*** then ***Store*** to confirm.

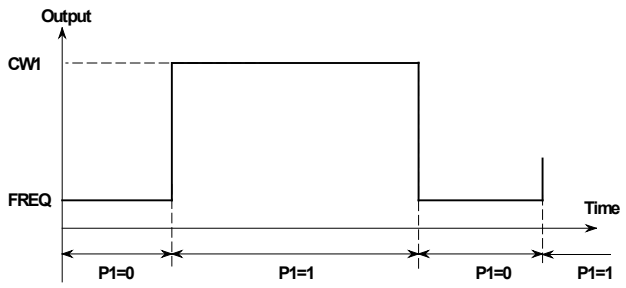
Press ***Write*** to load new values or when **Psel** state is changed

d) ***Step mode*** is a two level sweep. It is essentially the same as 2–level modulation (see section 2.4)



Step mode may be applied to the Frequency, Amplitude or Phase.
In the example screen shot above, frequency will switch between 69.5 and 110.5MHz
Also ***Full scale*** amplitude selected. ***Dwell / No dwell*** has no function.

(Plots shows a frequency step sweep for Ch1 controlled using input P1)



2.4 **Multi-level modulation.** Typical mode for AOTF applications.

The DDS chip contains 16 “profile” registers. These can be programmed to provide up to 16 levels of “modulation”. EITHER frequency, amplitude or phase can be “modulated” in any one RF channel.

The maximum number of levels per output is given by the relatonship:

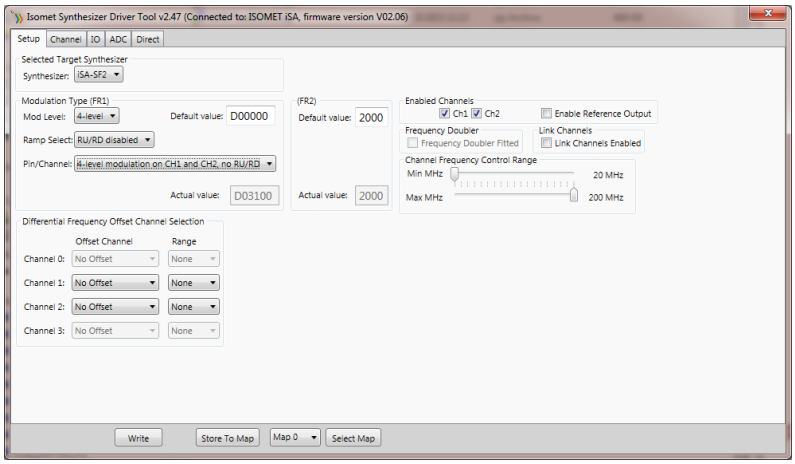
$$2^{(\text{Active channels})} \times \text{modulation levels} = 16$$

a) Under ***Setup** tab*, refer to the ***Modulation Type (FR1)*** panel
Example: 4-level frequency control on Channel 1 and Channel 2

Mod Level pull down menu, select ***4-level***

Ramp Select pull down menu, leave at ***RU/RD disabled***.
(If enabled, introduces automatic amplitude ramping of the DDS output)

Pin/Channel pull down menu, select the ***4-level modulation of Ch1 and Ch2***
(Ch0 and Ch3 are not available)

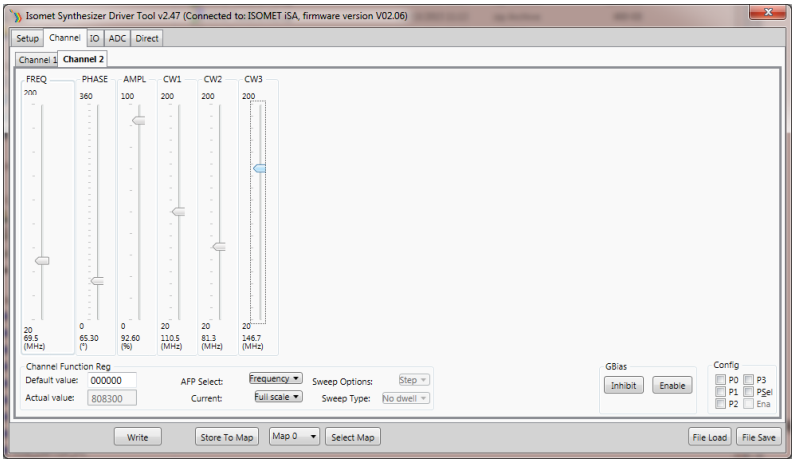


[Don’t forget, press ***Write*** to load new values]

b) Select the ***Channel*** tab

For **Channel 2** , set ***AFB Select*** to ***Frequency***
An additional 3 wipers will be displayed, allowing a total of 4 frequencies to be set.

Adjust sliders to desired values.



Repeat for ***Channel 1*** if required for a dual channel model

[Don't forget, press ***Write*** to load new values]

c) Output control

The driver output responds to the frequency modulation levels (i.e. the frequency selection values) by means of the 4 profiles inputs P0,1,2,3

Modulation Level	Profile Control	Active Channels
16-Level	P0 = MSB	Ch2 or Ch1
	P1	
	P2	
	P3 = LSB	
8-Level	P0 = MSB	Ch2 or Ch1
	P1	
	P2 = LSB	
	P3 = X	
4-Level	P0 = MSB	Ch2
	P1 = LSB	
4-Level	P2 = MSB	Ch1
	P3 = LSB	

The ***Psel*** check box selects the source for ***P0,P1,P2,P3*** modulation control signals.

Psel checked (high), selects external inputs on the 25way D-type (see page 21)

Psel unchecked (low), selects USB control via the *P0…P3* check boxes within the *Config* panel under the *IO* tab.

Press ***Write*** to load new values or when **Psel** state is changed

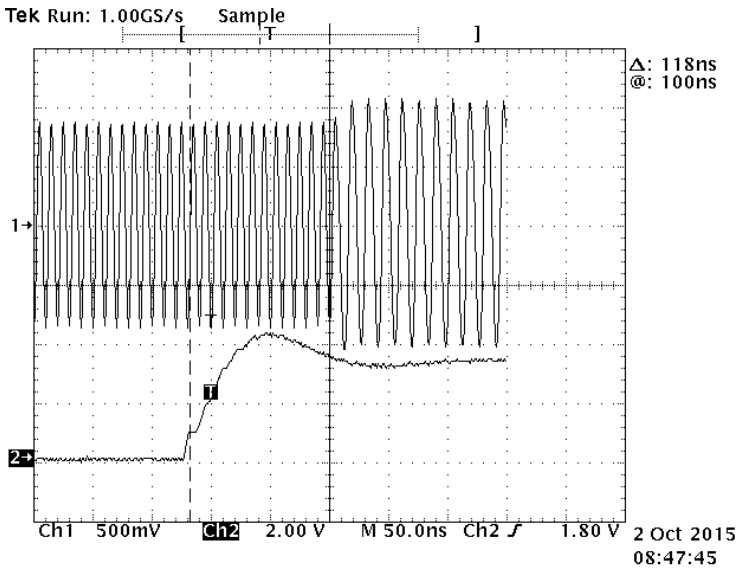
2.5 Profile Control Characteristics

For the Sweep and Multi–level modulation modes, the output responds to a change initiated by the profile control inputs within 100nsec. The DDS register data is volatile. See section 3 for storage.

Example output

Lower trace 2 is external ***P0, (or P1,P2,P3)*** modulation control signal.

Upper trace 1 is the RF output



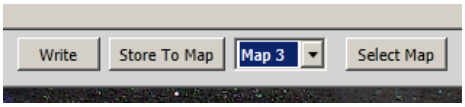
2. Data storage.

The iSA / iSPA drivers utilize the uC Flash memory for non-volatile storage of data.
The user can select up to 8 Maps to store all the DDS registers, including frequency, phase, amplitude and configuration data. The digital pots feature separate Flash storage and thus DAC wipers values are not stored in the MAP.

Data stored in MAP0 is always loaded on power-up or after a RESET is applied.

3.1 MAP Recall

Note: The GUI sliders do not change when the DDS registers are updated using MAP recall.



a) Recall via GUI: Use pull down menu to select MAP for recall e.g. Map 3

Press ***Select Map***
DDS registers will be updated and output will change to reflect the MAP3 data.
The registers can be viewed under the ***Direct*** tab.
For s/w control, ensure no external connections to pins 9,10,11,12 (see below)

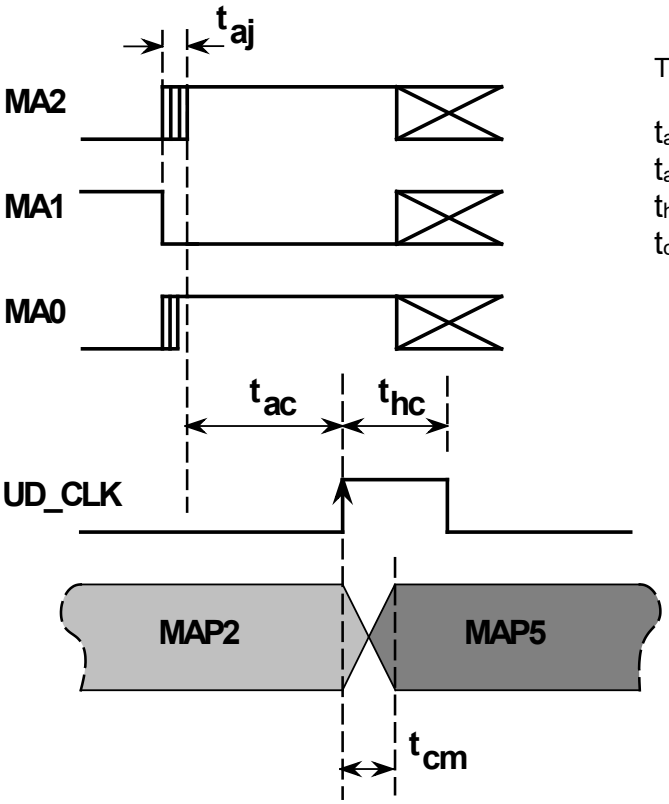
b) Recall using External control.

MAP data output can be synchronised to connected equipment using the MA address and UD_CK clock inputs on the 25-way D-type connector

External MAP selection

	Map Address Bit		
Data set	**MA2**	**MA1**	**MA0**
MAP7	1	1	1
MAP6	1	1	0
MAP5	1	0	1
MAP4	0	1	0
MAP3	0	1	1
MAP2	0	1	0
MAP1	0	0	1
MAP0	0	0	0
	Connector pin		
Address Bit Pins	9	10	11
Update Clock (UD-CK)	12		

Update response is determined by data transfer from uC Flash to DDS. The uC compares registers in MAP(n) and compares with MAP(n+1) in the sequence. Only registers with a data change are written to the DDS. This process will range from 50-100us depending on the register contents between adjacent MAPs in the sequence.



Timing:

t_{aj} Address edge jitter: <100nsec
t_{ac} Address settling time to clock edge: >55usec
t_{hc} UD-CLK pulse width: >100nsec
t_{cm} Clock edge to DDS output settling time: <100nsec

3. LED Indicator and Monitor outputs

The two front panel tri-colour LED sets indicate the operating state.

LED1	LED2
C	F
B	E
A	D

RED - A: **Normal condition is ON**
The bottom left LED will illuminate RED when DC power is applied.

YELLOW – B: **Normal condition is ON**
The middle left LED will illuminate YELLOW when the Power amplifier stages are enabled.

GREEN – C: **Normal condition is ON**
The top left LED: reserved for future use.

RED – D: **Normal condition is OFF**
The bottom right LED will illuminate RED when there is a fault condition.
This signal is also available on pin 8 of the 25way D-type connector. See STATUS MONITOR below
Fault conditions:
- DC power is below 15Vdc or above 28Vdc
- Over temperature fault

YELLOW – E: **Normal condition is ON**
The middle right LED will illuminate YELLOW when the DC supply voltage is within limits
Limits: 28V> v >15V.

GREEN – F: **Normal condition is OFF, not blinking**
The top right LED will blink GREEN when driver temperature is outside recommended limits
Limits: 50°C > T > 7°C.

RESETTING
Once the fault condition is corrected, it will be necessary to reset the driver.
1) Turn the DC power OFF and ON
or
2) RESET the driver by momentary connecting pin 13 of the D-type to pin 25

Status Monitor Output
The status of the RED-D LED is replicated at the D-type connector
“FAULT” = logic low between pins 8 and 21 = LED on
“OK” = logic high between pins 8 and 21 = LED off

Signal is LVTTL compatible. Sink / Source 4mA

5 INSTALLATION AND ADJUSTMENT

5.1 With no DC power applied, connect the + DC live to the center terminal of the feed-thru terminal. DO NOT APPLY POWER.

5.2 Connect the SMA RF connector(s) to the acousto-optic modulator RF input(s) or a 50Ω RF load if it is desired to measure the RF output power.

5.3 Drivers may be supplied with the optional Interlock connector (mini 4-pin snap type). This can be connected to the Interlock of the acousto-optic modulator.

5.4 Adjustment of the RF output power is best done with the driver connected to the acousto-optic device. Unless stated, the driver is shipped with the output power set to give 250mW maximum per output at 80MHz.

5.5 The optimum RF power level required for the modulator to produce maximum first order intensity will be differ depending in the laser wavelength. Applying RF power in excess of this optimum level will cause a decrease in first order intensity (a false indication of insufficient RF power) and makes accurate Bragg alignment difficult. It is therefore recommended that initial alignment be performed at a low RF power level.

5.6 The initial alignment should be made at the AO centre frequency at half RF power.

Using the GUI and no external inputs:

- Apply the DC supply voltage.
- Ensure there are no connections to 25 way D-type connector

Referring to the single tone basic setup described above;

- Tune the iSA / iSPA frequency to match the AO centre frequency using the ***FREQ*** slider
- Adjust the RF power by setting the ***AMPL*** slider to 30%

5.7 Input the laser beam toward the centre of either aperture of the AOM. Ensure the polarization is correct for the AO crystal and the beam height does not exceed the active aperture height of the AOM. Start with the laser beam normal to the input optical face of the AOM. See Figures 6 for the possible configurations.

Observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. Adjust the input angle (rotate the modulator) very slightly to maximise the first order beam intensity.

After the input angle has been optimized, slowly increase the RF power by increasing the AMPL slider until maximum intensity is obtained in the first order.

6 MAINTENANCE

Cleaning

It is of utmost importance that the optical apertures of the deflector optical head be kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

It will probably be necessary in time to wipe the coated window surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

Repairs

In the event of deflector malfunction, discontinue operation and immediately contact the manufacturer or his representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.

7. **Connection Summary** 25 way 'D' Type

Signal (see notes)	Type	Pin out connection
-OHL External Modulation Enable LVTTL high (1.9v<V<3.3v) or nc = Disable LVTTL low (0.0v<V<0.8v) = Enable	Input	Signal pin 7 Return pin 20
***(Ch 0) / P0** Control* *LVTTL levels (0.0v<V<3.3v)*	*Input*	*Signal pin 4* *Return pin 17*
Ch1 / P1 Control LVTTL levels (0.0v<V<3.3v)	Input	Signal pin 3 Return pin 16
Ch2 / P2 Control LVTTL levels (0.0v<V<3.3v)	Input	Signal pin 2 Return pin 15
***(Ch3) / P3** Control* *LVTTL levels (0.0v<V<3.3v)*	*Input*	*Signal pin 1* *Return pin 14*
MOD_A (-OHL=0 selects) 0 – 5V max	Input	Signal pin 6 Return pin 19
An_In external ADC input 0 – 10V max	Input	Signal pin 5 Return pin 18
OPTIONAL		
'**Status**' monitor (LVTTL compatible, Low = Fault) Maximum current = 4mA	Output	Signal pin 8 Return pin 21
-RESET , Active low. LVTTL levels (0.0v<V<3.3v) Internal pull up to +3v3 via 10Kohm	Input	Signal pin 13 Return pin 25
MA0, Map address bit0 *LVTTL levels (0.0v<V<3.3v)*	Input	Signal pin 11 Return pin 24
MA1, Map address bit1 *LVTTL levels (0.0v<V<3.3v)*	Input	Signal pin 10 Return pin 23
MA2, Map address bit2 *LVTTL levels (0.0v<V<3.3v)*	Input	Signal pin 9 Return pin 22
UD_CK, MAP Update Clock LVTTL positive edge (0.0v< V<3.3v)	Input	Signal pin 12 Return pin 25

NOTES:
Pins 14 to 25 are internally connected to 0V

Example external connections

Connection for Ramp mode and External amplitude control

- Ext'l Modulation Control
- Mod_A , modulation
- Ch1 (P1) and Ch2 (P2) ramp control

Also

- Reset
- An_In, ADC user input

Connection for Multi-level mode and MAP select

- Profile inputs
- MAP select
- UD-CK

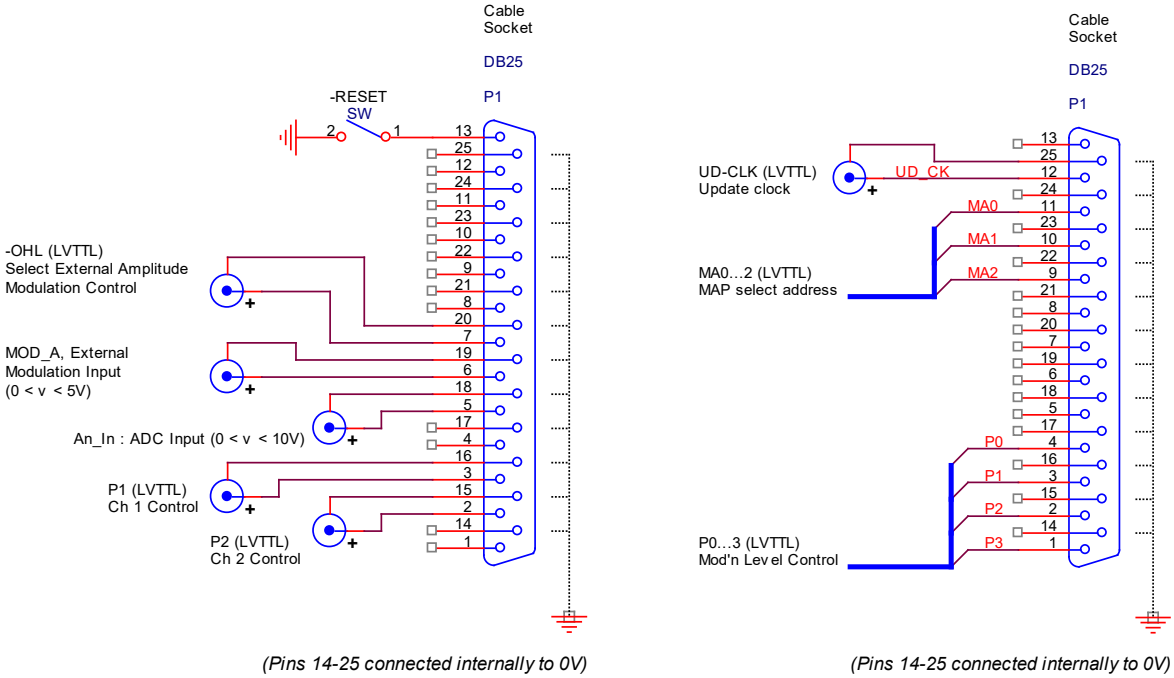


Figure 3:

Notes:

* External connection to the 25way D-type is not necessary for driver operation

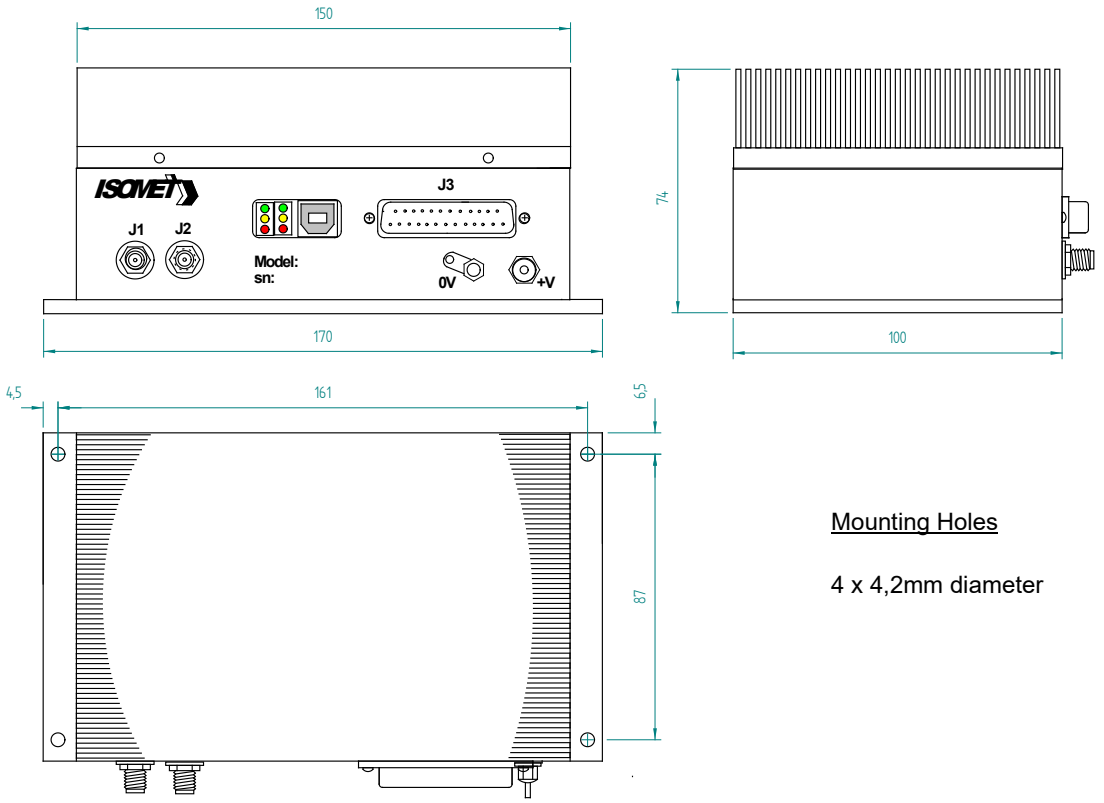


Figure 4a: Driver Installation, iSPA style shown with finned heat sink
Ensure free air flow around heat sink or use forced air

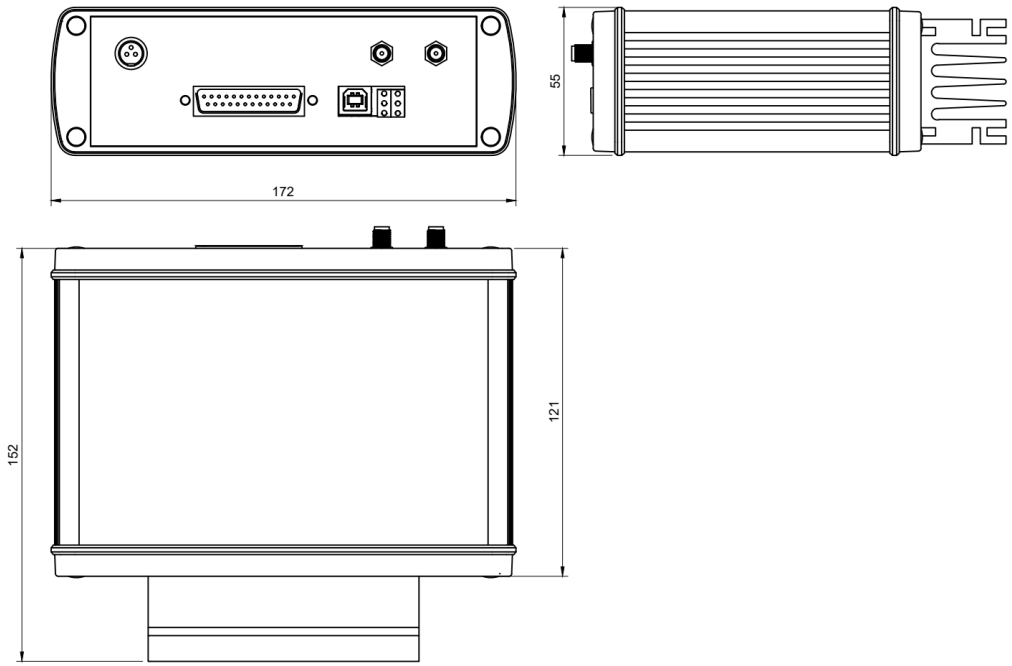


Figure 4b: Driver Installation, iSPH- style case shown with finned heat sink
Ensure free air flow around heat sink or use forced air

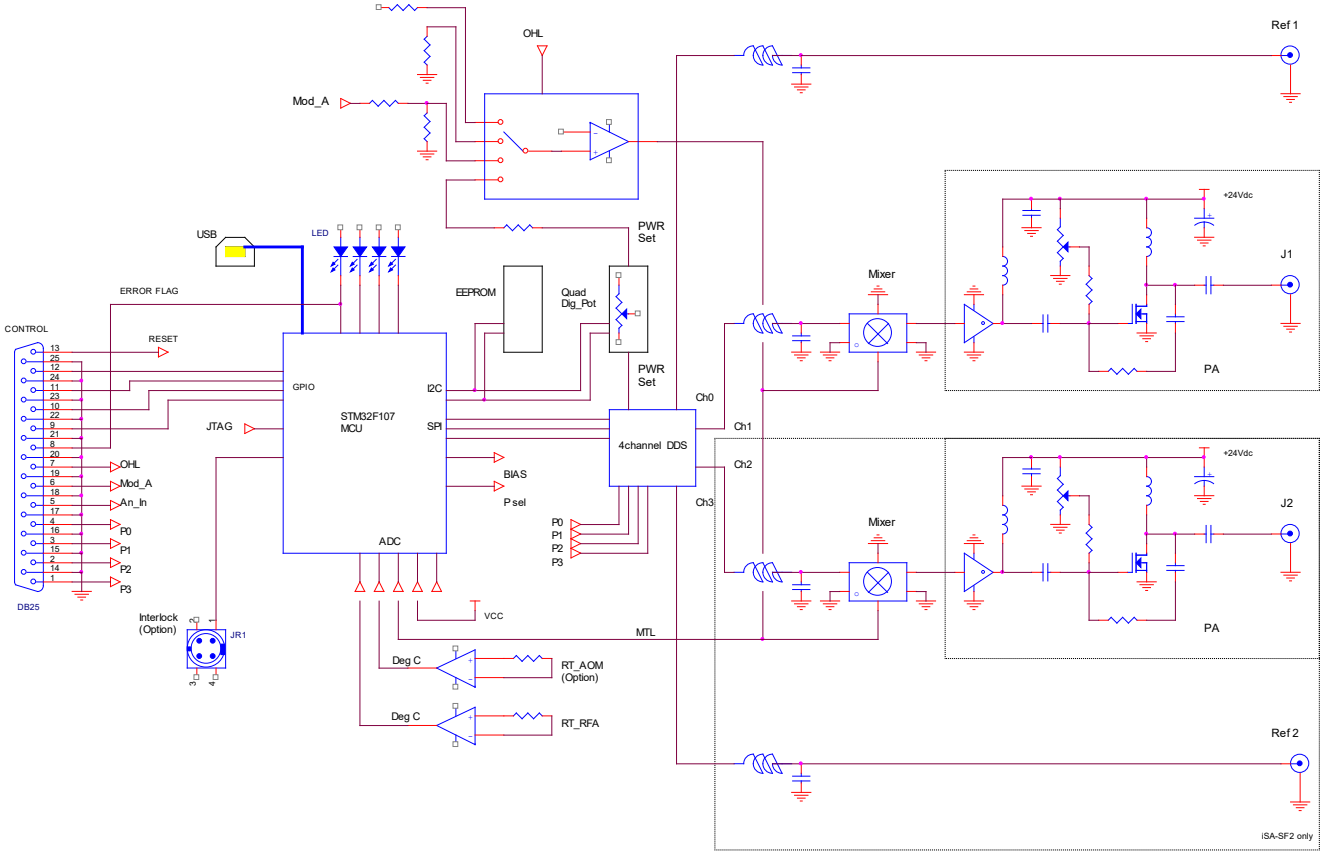
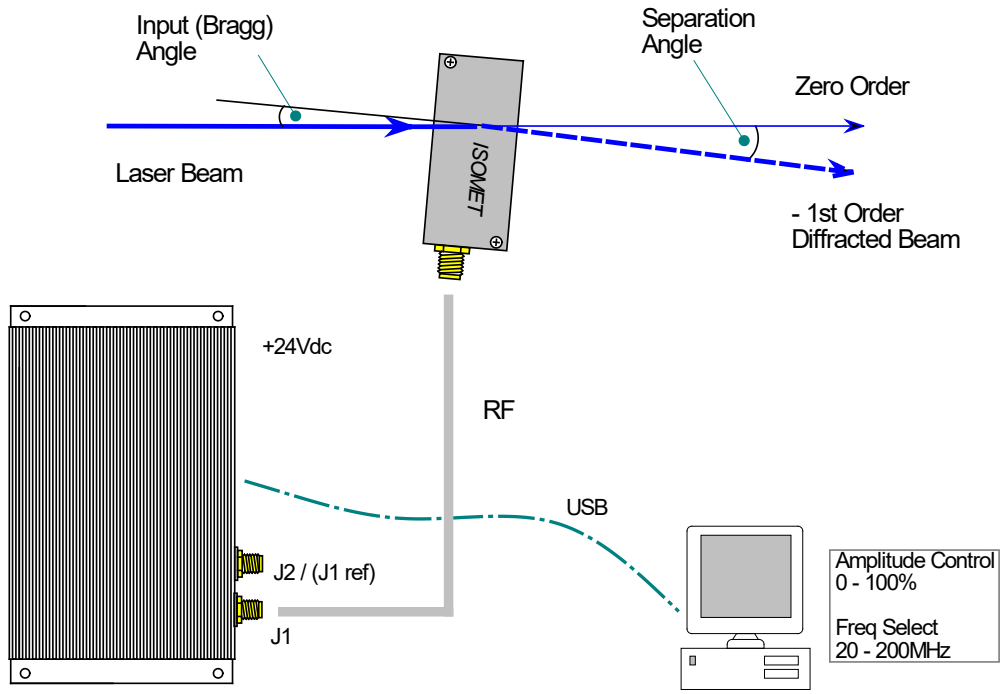


Figure 5: Driver Block Diagram

8. AOM/AOD Set-up

Typical AOM configuration
As shown, operating in -Bragg Condition



The input Bragg angle relative the optic face normal is:

$$\theta_{Bragg} = \frac{\lambda.fc}{v}$$

The separation angle between the Zeroth order and the First order is:

$$\theta_{SEP} = \frac{\lambda.fc}{v}$$

Optical rise time for a Gaussian input beam is approximately:

$$t_r = \frac{0.65.d}{v}$$

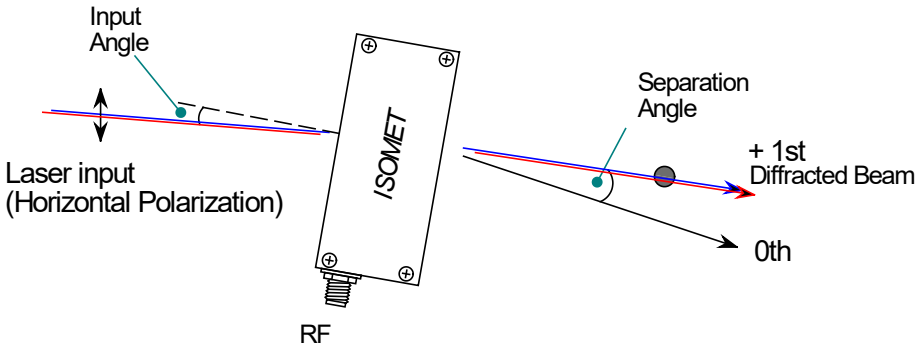
where: λ = wavelength
fc = centre frequency
v = acoustic velocity of AO interaction material = 4.21mm/usec (TeO_2)
= 3.63mm/usec ($PbMoO_4$)
= 5.7mm/usec (Quartz)

d = $1/e^2$ beam diameter

9. Basic AOTF Set-up

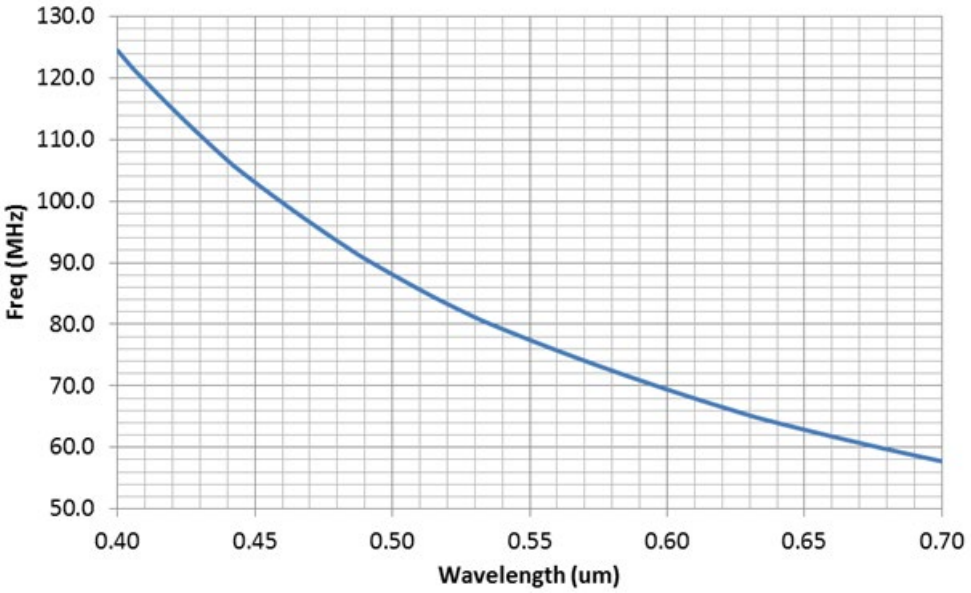
Initial alignment is best accomplished using a source of known wavelength e.g. 488nm or 633nm laser and a driving at a constant RF frequency.

Please refer to the specific AOTF data and test sheets.
Generic schematic



Input the light source and rotate the AOTF so that the incident beam is in the correct orientation and angle. Ensure the light beam is in the centre of the aperture. Start with the input beam at normal incidence. A slight rotation such that the beam is directed away from connector end of the AOTF will avoid back reflection into the source

Select the drive frequency. This depends on the input laser wavelength. Refer to the AOTF 'Tuning Characteristic' graph supplied with the device. A typical plot will look as shown below



Adjust the ***FREQ*** slider to enter the corresponding frequency

Assuming 633nm is used for this initial alignment, set the FREQ slider to frequency of ~ 64MHz

Apply approximately half the required RF power (say 0.1W) at the desired frequency.
This is achieved by adjusting the AMPL slider setting to approx. 10%.

NOTE: AOTF's are generally very efficient and require low RF driver powers.
e.g. ~ 100mW at visible wavelengths
Take care not to overdriv.e

The diffraction will occur in the horizontal plane. There will be several output beams

For un-polarized light, select one of the two strong spots diffracted either side the zero order.
For a polarized input, there will be only one significant diffracted spot.

NOTE: Some models are polished to negate chromatic dispersion and thus maintain a constant output beam angle with tuned wavelength. This characteristic only applies for a given input polarization. Refer to model data sheet .

In all cases, the polarization of the output diffracted beams will be rotated by 90°.

Monitor the light intensity by using either a photodetector or a light power meter

Adjust the (input) angle to give the maximum output power. Use the smallest input angle possible.
If necessary, make minor RF frequency adjustments to peak the efficiency. The peak should be around 40-50%.

AFTER the angle and frequency have been optimized, then increase the RF power slowly to maximize the diffraction efficiency.

Do NOT exceed the RF power level at which maximum efficiency is achieved (Psat).

CAUTION: Over driving the AOTF will reduce efficiency, increase the filter side-lobes, increase thermal dissipation and may result in serious damage to the AO crystal.